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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,309	11/17/2003	Ketan Padalia	015114-069200US	6902

26059 7590 05/22/2006

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5/1

Office Action Summary	Application No.	Applicant(s)	
	10/716,309	PADALIA ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/23/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' amendment to 10/716,309 has been examined. The specification has been amended. Claims 1, 9, 12, 14, 16-17 and 21-23 have been amended. Claims 27-29 have been added. Claims 1-29 are pending.

Applicants' amendment is considered persuasive in part and the applicable rejections from the prior office action along with new ground of rejection are incorporated herein.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-29 are rejected under 35 U.S.C. 103(a)** as being unpatentable over DiGiacomo et al. (US Patent No. 4,630,219). DiGiacomo teaches circuit elements (col. 6, line 30-33). DiGiacomo does not explicitly teach abstract blocks and logic blocks. However, DiGiacomo does teach macros (col. 1, line 25-26) and clusters (col. 11, line 30-38) that are similar to abstract blocks and logic blocks. Therefore, it would have been obvious to one of ordinary skill in the art at the time with invention was made to use the macros and clusters taught by DiGiacomo as abstract blocks and logic blocks since DiGiacomo teaches that their functions are essentially the same.

As per **claim 1**, DiGiacomo discloses a method for placing circuit elements (col. 1, line 28-30; where elements are circuit elements) into logic blocks (col. 11, line 30-38; where clusters are logic blocks), the method comprising:

assigning each of the circuit elements to a separate abstract block (col. 1, line 25-26; where macros are abstract blocks), wherein the circuit elements are part of a user design for a programmable integrated circuit (col. 2, line 44-50) and the abstract block represents a functional attribute of its assigned circuit element (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38);

grouping each of the abstract blocks into a logic block (col. 2, line 50-54) based at least in part on a correspondence between a functional attribute of the logic block and the functional attribute of each abstract block (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38);

removing a first one of the abstract blocks from a logic block in response to placement information that indicates a design goal would be improved by rearranging at least a portion of the user design (Fig. 13; Fig. 46A; Fig. 46B; col. 9, line 43-59;); and

placing the first abstract block into a different logic block on the programmable integrated circuit (col. 29, line 27-43; col. 29, line 50-57), wherein the functional attribute of removed abstract block corresponds with a functional attribute of the different logic block (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38);

As per **claim 2**, DiGiacomo discloses the method according to claim 1 wherein the design goal includes routability and signal timing in the user design (col. 8, line 3-10; col. 8, line 13-28).

As per **claim 3**, DiGiacomo discloses the method according to claim 1 wherein the circuit elements include lookup tables and registers (col. 1, line 24-28; col. 6, line 59-64, where circuit elements can include integrated circuit lookup tables and registers).

As per **claim 4**, DiGiacomo discloses the method according to claim 1 wherein the circuit elements include DSP blocks and RAM blocks (col. 1, line 24-28; col. 6, line 59-64, where circuit elements can include integrated circuit DSP blocks and RAM blocks).

As per **claim 5**, DiGiacomo discloses the method according to claim 1 further comprising:

determining whether placing each circuit element into the logic block violates any of a set of design rules relating to the logic block, wherein the logic blocks are grouped into clusters (Fig. 1, #12, #13; col. 6, line 25-42; Fig. 2, #22; col. 7, line 7-16); and

determining whether placing each of the circuit elements into a cluster violates any of a set of design rules relating to the cluster (Fig. 2, #22; Fig. 17; col. 11, line 51-53; col. 11, line 22-38, where the designs rules are the connectivity matrix).

As per **claim 6**, DiGiacomo discloses the method according to claim 5 wherein each of the abstract blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and the attraction measures a number of nets and

connections of nets absorbed into the cluster if the abstract block is placed inside the cluster (col. 8, line 3-12; col. 12, line 25-28; col. 28, line 12-16).

As per **claim 7**, DiGiacomo discloses the method according to claim 5 wherein each of the abstract blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and the attraction measures a number of timing critical connections absorbed into the cluster if the abstract block is placed inside the cluster (col. 3, line 47-68; col. 4, line 1-7; col. 8, line 3-10; col. 28, line 12-16).

As per **claim 8**, DiGiacomo discloses the method according to claim 5 further comprising:

placing one of the abstract blocks into another logic block within the cluster if placing that abstract block into the logic block violates any of the design rule relating to the logic block (col. 38, line 14-28; col. 11, line 22-38, where the design rules are the connectivity matrix), and

placing one of the abstract blocks into another cluster if placing that abstract block into the cluster violates any of the design rules relating to the cluster (col. 13, line 17-29; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 9**, DiGiacomo discloses the method according to claim 1 wherein the logic blocks implement functions performed by two lookup tables with less than an integer k unique input variables (col. 10, line 41-50); and the method further comprises:

determining whether grouping each of the abstract blocks into the logic block causes any of the logic blocks to have more than k unique input variables (Fig. 6; col. 7, line 65-68; col. 8, line 1-3).

As per **claim 10**, DiGiacomo discloses the method according to claim 1 wherein the placement information includes floorplanning information (Fig. 9; col. 9, line 27-31).

As per **claim 11**, DiGiacomo discloses the method according to claim 1 wherein the placement information includes partition information (Fig. 17, #15; Fig. 21; Fig. 19B; col. 14, line 30-53).

As per **claim 12**, DiGiacomo discloses the method according to claim 1 wherein the placement information includes data obtained by a previous placement of a portion of the user design on the programmable integrated circuit (Fig. 22, #82, #83; col. 15, line 19-30; col. 21, line 66-68; col. 22, line 1-22).

As per **claim 13**, DiGiacomo discloses the method according to claim 1 wherein:

grouping each of the abstract blocks into a logic block further comprises grouping first and second abstract blocks into a first logic block:

removing the first one of the abstract blocks from the logic block further comprises removing the first abstract block from the first logic block (col. 3, line 26-46; col. 4, line 8-17); and

placing the first abstract block into a different logic block further comprises placing the first abstract block into a second logic block and placing the second abstract block into the first logic block (col. 4, line 18-30).

As per **claim 14**, DiGiacomo discloses a computer program product stored on a computer readable medium for placing circuit elements in a user design for a programmable integrated circuit into logic blocks (Fig. 1, #14, #16; col. 1, line 6-13; col. 6, line 19-24), the computer program product comprising:

computer program instructions for assigning each of the circuit elements to a separate abstract block (col. 2, line 44-50), wherein the abstract block represents a functional attribute of its assigned circuit element (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38);

computer program instructions for grouping each of the abstract blocks into a logic block (col. 2, line 50-54) based at least in part on a correspondence between a functional attribute of the logic block and the functional attribute of each abstract block (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38);

computer program instructions for determining whether placement information indicates that a design goal would be improved by moving at least one of the abstract blocks into a different logic block (col. 29, line 27-43; col. 29, line 50-57); and

computer program instructions for removing the at least one abstract block from a first logic block and placing the at least one abstract block into a second logic block in response to the determination based on the placement information (Fig. 13; Fig. 46A; Fig 46B; col. 9, line 43-59), wherein the functional attribute of the removed abstract block corresponds with a functional attribute of the different logic block (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38).

As per **claim 15**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the design goal includes signal timing and routability in the user design (col. 8, line 3-10; col. 8, line 13-28).

As per **claim 16**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the logic blocks are grouped into clusters of logic blocks, and the

computer program instructions for grouping each of the abstract blocks into a logic block further comprises computer program instructions for grouping each of the abstract blocks into a cluster of logic blocks based on an attraction of the abstract block to the cluster (col. 8, line 3-12; col. 12, line 25-28; col. 28, line 12-16).

As per **claim 17**, DiGiacomo discloses the computer program product as defined in claim 16 further comprising:

computer program instructions for determining whether grouping the abstract blocks into the clusters violates any design rules of the clusters (col. 13, line 17-29; col. 11, line 22-38, where the design rules are the connectivity matrix); and

computer program instructions for determining whether grouping the abstract blocks into the logic blocks violates any design rules of the logic blocks (col. 38, line 14-28; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 18**, DiGiacomo discloses the computer program product as defined in claim 14 wherein some of the circuit elements are lookup tables, and some of the circuit elements are registers (col. 1, line 24-28; col. 6, line 59-64, where circuit elements can include integrated circuit lookup tables and registers).

As per **claim 19**, DiGiacomo discloses the computer program product as defined in claim 16 wherein the attraction measures a number of nets and connections of nets absorbed into the cluster if the abstract block is placed inside the cluster (col. 8, line 3-12; col. 12, line 25-28; col. 28, line 12-16).

As per **claim 20**, DiGiacomo discloses the computer program product as defined in claim 16 wherein the attraction measures a number of timing critical connections

absorbed into the cluster if the abstract block is placed inside the cluster (col. 3, line 47-68; col. 4, line 1-7; col. 8, line 3-10; col. 28, line 12-16).

As per **claim 21**, DiGiacomo discloses the computer program product as defined in claim 17 further comprising:

computer program instructions for placing one of the abstract blocks into another logic block if placing that abstract block to the logic block violates any of the design rules relating to the logic block (col. 38, line 14-28; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 22**, DiGiacomo discloses the computer program product as defined in claim 17 further comprising:

computer program instructions for placing one of the abstract blocks to another cluster if placing that abstract block to the first cluster violates any of the design rules relating to the first cluster (col. 13, line 17-29; col. 11, line 22-38, where the design rules are the connectivity matrix).

As per **claim 23**, DiGiacomo discloses the computer program product as defined in claim 14 further comprising:

computer program instructions for determining whether placing the abstract blocks to the logic blocks causes any of the logic blocks have more than k unique input variables (col. 10, line 41-50),

wherein the logic blocks are configurable to implement functions performed by two lookup tables with less than k unique input variables (Fig. 6; col. 7, line 65-68; col. 8, line 1-3).

As per **claim 24**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the placement information includes floorplanning information (col. 3, line 44-50).

As per **claim 25**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the placement information includes partition information (col. 21, line 9-26).

As per **claim 26**, DiGiacomo discloses the computer program product as defined in claim 14 wherein the placement information includes data obtained by placing logic blocks that implement portions of the user design on the programmable integrated circuit (Fig. 22, #82, #83; col. 15, line 19-30; col. 21, line 66-68; col. 22, line 1-22).

As per **claim 27**, DiGiacomo discloses the method of claim 1, wherein the logic block includes a first functional attribute and a second functional attribute, and wherein grouping each of the abstract blocks into a logic block further comprises:

Assigning a first abstract block associated with a first circuit element to the first functional attribute of the logic block (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38); and

Assigning a second abstract block associated with a second circuit element to the second functional attribute of the logic block, such that the logic block is assigned the functional attributes of the first and second circuit elements (col. 1, line 24-28; col. 1, line 45-47; col. 11, line 35-38).

As per **claim 28**, DiGiacomo discloses the method of claim 27, wherein the first functional attribute of the logic block includes a register and the functional attribute of

the first circuit element includes a register (col. 1, line 24-28; col. 1, line 45-47; col. 6, line 59-64; col. 11, line 35-38; where circuit elements can include integrated circuit registers).

As per **claim 29**, DiGiacomo discloses the method of claim 27, wherein the second functional attribute of the logic block includes a look-up table circuit adapted to implement a logic function and the functional attribute of the first circuit element includes a logic function capable of being implemented by the look-up table circuit (col. 1, line 24-28; col. 1, line 45-47; col. 6, line 59-64; col. 11, line 35-38; where circuit elements can include integrated circuit look-up table).

Remarks

4. Applicants state the DiGiacomo does not consider the function of elements in determining their placement. The Examiner respectfully disagrees and refers applicants to column 1, lines 24-28, column 1, line 45-47 and column 11, lines 35-38 of DiGiacomo. Column 1, lines 24-28 states, "The elements to be placed may be macros, i.e., a group of related circuits for performing a given function...". Column 1, lines 45-47 and column 11, lines 35-38 refers to placement which take into consideration input/output connections, test points and the process of clustering and ordering highly interconnected components. These considerations suggest that DiGiacomo considers the function of elements or components when performing placement since reducing the amount of wiring needed to connect signal nets is commonly performed when placing elements that are similarly related in function. Therefore, from the previous office action and instant action, the rejections of DiGiacomo are maintained.

Upon reconsideration herein, Examiner has determined the rejection under 35 USC 103(a) as appropriate. Therefore, the amended and instant rejection has established a solid prima facie case of obviousness.

Examiner had originally intended a rejection under 35 USC 102(b). Therefore, no motivation statement was provided as part of the rejection. Examiner regrets any confusion caused by the omission.

Conclusion

5. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson Lam

Nelson Lam
Assistant Examiner
Art Unit 2825

A. M. Thompson
Primary Examiner
Technology Center 2800